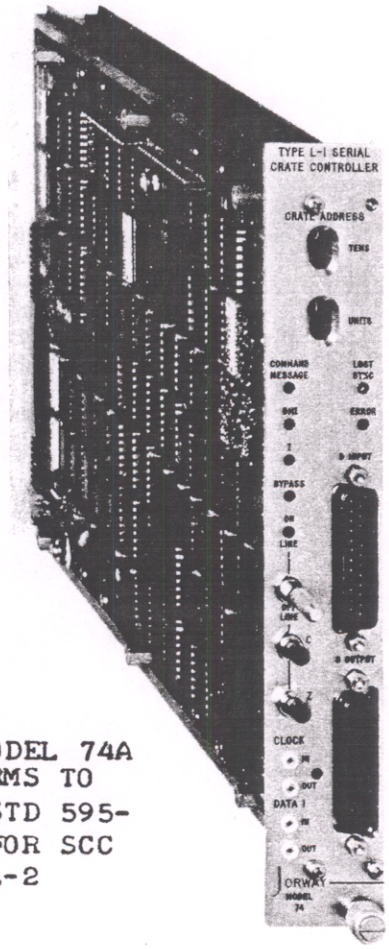
MODEL 74

TYPE L-1 SERIAL CRATE CONTROLLER

The Jorway Model 74 Type L-1 Serial Crate Controller interfaces the Dataway of a Camac crate with the standard Serial Highway which is described in TID-26488 (Esone SH/01). The Type L-1 controller, incorporating virtually all of the numerous features detailed in the description, significantly enhances the versatility of the Serial System. Many of these features are not necessarily provided in othe types. The Serial Highway, when implemented with the Model 74 controller, providea many advantages over previously available Camac systems. Among these are:

- LARGE SYSTEMS CAN BE ASSEMBLED...Up to sixty-two crates accommodated in a single serial loop.
- LONG DISTANCE LINKS BETWEEN CRATES...Considerable distance with direct connections, unlimited distance using suitable communications channel.
- BOTH BIT AND BYTE SERIAL...User can select bit serial for simpler, more economical cabling, byte serial for maximum speed.
- HIGH DATA RATE CAPABILITY...Up to 5Mbits/s in bit serial mode, 5Mbyte/s in byte serial mode.
- EFFICIENT DEMAND HANDLING...Demand messages are spontaneously generated by controller when attention is required, repeated Demands sent until serviced.
- PROVISION FOR AUXILLIARY CONTROLLERS...Autonomous controllers can control Dataway on a time shared basis.



THE MODEL 74A CONFORMS TO IEEE STD 595-1976 FOR SCC TYPE L-2

GENERAL DESCRIPTION

The Model 74 accepts and transmitts messages of the types, formats, and sequences as described in TID-26488. Both bit and byte mode operation are provided at clock rates up to 5MHz. The geometric error detection scheme and byte and message synchronization methods described are also implemented. Dataway common control signals as well as a number of special instructions to the controller itself are handled by an internal status register.

The front panel contains a number of indicators which provide information relating to the operation of the controller. Additionally, the front panel has a switch to enable an "OFF LINE" state and pushbuttons for manually generating Dataway Clear (C) and Initialize (Z) when in this state. Two multipin connectors are provided on the front panel (one input and one output) for access to the serial highway and a Graded-L (SGL) connector on the rear panel permits connection to an external SGL encoder. Crate address asignment is set by a two digit decimal switch accessable through the front panel. Visual indication of the crate number is provided via windows in the front panel.

Data is received and transmitted via the unit's "D" (Defined) ports. These are multipin connectors located on the front panel of the Model 74. The data and clock inputs/outputs conform to the required signal standards for Serial Highway D ports. Eight data line pairs are provided for the byte data. When operating in bit mode data bit #1 is used for the single data line. An additional pair is provided for the clock which is used in both bit and byte mode.

The clock signal is automatically regenerated by the Model 74 so that both lobes of the clock waveform are always transmitted with a minimum width maintained regardless of the shape of the input waveform. This prevents the cumulative effect of passing through successive controllers from degrading the clock to a point at which it is outside of the limits required for proper controller operation. This is important for system operation at or near the maximum clock frequency.

Selection of bit or byte serial mode is made via an internal programing plug which the user places in the appropriate position.

Internally, the Model 74 processes all messages in byte format. When operating in the bit mode, data received on the single data input line is shifted serially into the input register by the bit clock. Once byte synchronization is acquired, an input byte clock is derived from the stop bit of each byte. Each input byte clock signals that a complete byte has been loaded into the register, whereupon the byte is processed.

In the byte mode data is received in byte format over the eight input data lines. The input byte clock is used to strobe incoming data at a time that it is guaranteed to be stable. It is then stored in the unit's input register. The reverse process takes place for output data. In the bit mode of operation, a parallel to serial converter serializes the output byte for transmission over the single output data line. An output byte clock derived from the start bit of the incoming data is used to initiate the output byte which is then shifted out of the unit's output register by the bit clock.

Output data in the byte mode is taken in parallel from the output register for transmission over the eight data output lines.

When power is applied to the crate, the controller automatically assumes all the necessary internal states so that it can respond to message traffic. Certain status register bits are set to defined states, and a Dataway Initialize operation is performed, to set all modules in the crate to their initial states.

A number of the Model 74's internal features are activated through its Status Register. Certain bits of the register can be both written into and read out, while others can be written or read only. Dataway common control lines C,Z, and I are generated by appropriate commands to the Status Register. While a command to write into the I Status Register sets (or clears) the bit in the usual way, commands to generate C or Z do not set a register bit, but rather initiate an appropriate Dataway Unaddressed Operation. Three other register bits, Dataway I, DOF Switch, and Selected LAMS Present, are not actual registers, but test the states of their respective inputs.

A Reread function is implemented in the Model 74. This command permits the recovery of data which may have been lost due to an error in transmission between the controller generating the data and the system driver. When the controller transmits the Read Field data in response to a read command, it retains that data in its registers. A command to Reread inhibits the read registers from being updated with new data and transmits the stored data. Thus, the Reread command presents data which is an exact duplicate of that data assembled for the preceding Read command. SQ in the status field of a Reread reply is set to the same state as DSQ indicating the Q response generated during the original Read Command. SQ, therefore reflects the validity of the Read field data being presented.

Both Bypass and Loop Collapse facilities are included in the Model 74. A control bus for each is provided in one of the D port connectors. The state of each control bus is determined by a corresponding status register bit which may be set or cleared on command. The user must furnish the external hardware to implement the appropriate switching.

The Model 74 may be placed in an Off-line mode which is useful for test and maintenance purposes. When in this mode Dataway operations are not executed, however commands to the Status Register are completed.

The Off-line mode may be selected either by command to set the DOF (Dataway Off line) Status Register bit, or manually from the front panel ON LINE/OFF LINE switch. The ON LINE indicator on the front panel is illuminated only when the Model 74 is in the On line state, i.e., the front panel switch is in the On line position and the Status Register DOF bit is reset. The controller responds to message traffic when in the Off line state, accepting commands and sending reply messages.

The Model 74 handles Demands in the manner described in the serial highway specification. A three-byte memory delays incoming messages during Demand Message transmission. A Status Register bit, Enable Demands, provides a means to enable/disable Demand Message generation. Another Status Register bit, Internal Demand, may be utilized to generate a Demand Message. This is useful as a method to test the proper operation of the Demand generation process. A connector located on the rear panel is provided to attach an optional external SGL(graded-L) encoder. All input and output signals required for the implementation of the encoder are contained in this connector.

A Demand Message is initiated,(but not necessarily immediately transmitted due to message traffic), by applying a logic "1" to the Demand Message Initiate(DMI) input in the SGL connector. The SGL field of the Demand Message will have data corresponding to the five SGLE (encoded output pattern from the encoder),if an encoder is used. If an encoder is not used, the SGLE inputs may be connected to a data source having any coding or significance which the user desires.

All Dataway L signals are brought out to the SGL connnector for use by the encoder. Additionally, the Model 74 provides a SUM output which is the logical or of all L signals, hence, will be active when one or more LAM requests are present.

An internal Repeat Timer is included in the Model 74. The timer is used to generate repeated Demand Messages if, for any reason, the original Demand is not acted upon(and LAM cleared) within a preset time interval. The Repeat Timer may be set for any interval between 1 millisecond and 10 seconds. Repeated Demand Messages are in the form of "Hung Demands". These are identified by the fact that they have all bits of their SGL field set to logic "1". The Repeat Timer is started by bringing the Start Timer (STIM) input to a logic "1", and will continue to cycle until this input is returned to logic "0". Each time the timer times out, a signal is produced at the Time Out (TIMO) output.

The Model 74 is designed so that an auxiliary controller may also control Dataway operations on a time sharing basis; i.e., when the Model 74 is not performing a Dataway operation in response to a Serial Highway command, the auxiliary controller, operating autonomously, may do so.

Such a controller, placed in any of the crate's normal stations, has access to all of the Dataway signals except for the N and L lines. By connection to the Model 74 through its SGL connector, the L lines can be directly accessed. The SGL connector also contains five "CODED N" inputs which are connected to the inputs to the Model 74's

N decoder. By addressing these lines (N1,N2,N4,N8, N16) any of the 24 N stations can be accessed. Thus, all Dataway lines are available to the auxiliary controller.

So that the two controllers may operate without conflict, the auxiliary controller must not generate commands onto the Dataway when the Model 74 is using the Dataway for an operation commanded from the Serial Highway.

An Auxilliary Controller Lockout signal is provided in the SGL connector which is active when the Model 74 is using the Dataway (or expects to do so shortly). The auxilliary controller uses this signal to inhibit initiation of a Dataway operation which may interfere with the execution of a command from the Serial Highway.

SPECIFICATIONS

FRONT PANEL CONTROLS	FUNCTION
OFF LINE switch	Selects OFF LINE state.
C pushbutton (effective when Off line only)	Generates Dataway cycle with C,S1,S2,B.
Z pushbutton (effective when Off line only)	Generates Dataway cycle with Z,S1,S2,B.
CRATE ADDRESS switch (tens and units)	Sets assigned crate number. Valid addresses are 00-62.
FRONT PANEL INDICATORS	**WHEN ILLUMINATED**
ON LINE	Controller is in the ON LINE state.
LOST SYNC *	Controller is not synchronized (Byte or Message).
COMMAND MESSAGE *	Controller has accepted a command addressed to it, and is engaged in a command-reply transaction.
ERROR *	A parity error has been detected by controller while receiving a message addressed to it.
BYPASS	Bypass Status Register is set.
I	Dataway Inhibit (I) line is at logic "1" from any source.
DMI	Demand Message Initiate input is at logic "1".

* indication is "stretched" so that short duration signals are visible.

FRONT PANEL CONNECTORS	USE
D INPUT	Serial Highway input port. 25 contact connector Cannon DBC-25P.
D OUTPUT	Serial Highway output port. 25 contact connector Cannon DBC-25S.

FRONT PANEL TEST JACKS	USE
CLOCK IN	Monitors the input clock signal.
CLOCK OUT	Monitors the output clock signal.
DATA 1 IN	Monitors the input data in bit mode, and data bit #1 (1sb) in byte mode.
DATA 1 OUT	Monitors the output data in bit mode, and data bit #1 (1sb) in byte mode.

NOTE: All test jack signals are TTL levels.

REAR PANEL CONNECTOR	USE
SGL connector	For attachment of optional SGL Encoder and/or Auxilliary controller. Also used for Repeat Timer connections. 52 contact connector Cannon 2DB52P.

INTERNAL CONTROLS	DESCRIPTION/USE
BIT-BYTE selector	A programming plug placed in the appropriate position selects Bit or Byte serial mode.
REPEAT TIMER RANGE selector	A programming plug placed in one of five positions selects the adjustable range of the internal Repeat Timer. Timer can be set to any time from 1ms to 10s.
REPEAT TIMER FINE ADJUSTMENT	A variable control to set the repeat timer to any time within the selected range.

D PORT SIGNALS	
Transmission mode	Bit or byte serial
Clock rate	0 to 5 MHz
Data coding	Non-return-to-zero
Clock propagation delay (input to output)	120 ns nominal
Inputs	Differential pair
Sensitivity	200 mv (line to line)
Common mode range	+7v to -7v
Input resistance	100Ω ±10% (line to line), ≥2KΩ (line to ground)
Outputs	Differential pair
Output voltage (line to line)	3v typical (open circuit), 2v minimum (terminated in 100Ω)
Output resistance	<100Ω (line to line)
Short circuit current	<150 ma (line to ground)
Signal rise and fall times	<20 ns (10% to 90%)

DATAWAY SIGNALS

Inputs				
Threshold voltage		+1.1v typical		
Pull-up capability		10.2 ma @ +0.5v		
Current source		2.6 ma @ +3.5v		
Outputs	R,Q,X,L	W,A,F,B,Z,C,I	N	S1,S2
Current sinking capability @ +0.5v		39.4 ma	7.6 ma	56.0 ma
Pull-up capability @ +3.5v		2.6 ma	2.6 ma	12.6 ma
Timing				
Cycle time		1.0 μs minimum, 1.5 μs maximum		
S1,S2 pulse width		200 ns minimum, 240 ns typical		

ERROR CONTROL

Transverse parity	Odd
Longitudinal parity	Even

COMMANDS

DATAWAY COMMAND	
READ STATUS REGISTER	N(30)A(0)F(1)
WRITE STATUS REGISTER	N(30)A(0)F(17)
SELECTIVE SET STATUS REGISTER	N(30)A(0)F(19)
SELECTIVE CLEAR STATUS REGISTER	N(30)A(0)F(23)
REREAD PREVIOUS READ FIELD	N(30)A(1)F(0)
READ LAM PATTERN	N(30)A(12)F(0)
ERROR REPLY TO ANY COMMAND	

RESPONSE	NORMAL		OFF LINE		BYPASSED	
	SQ	SX	SQ	SX	SQ	SX
	Q	X	0	0	1	0
	1	1	1	1	1	0
	1	1	1	1	1	0*
	1	1	1	1	1	0
	1	1	1	1	1	0*
	DSQ	1	DSQ	1	1	0
	1	1	0	0	1	0
	0	0	0	0	0	0

* Except command to clear Bypass, X=1

Note: If controller is both OFF LINE and BYPASSED, the responses shown for BYPASSED apply.

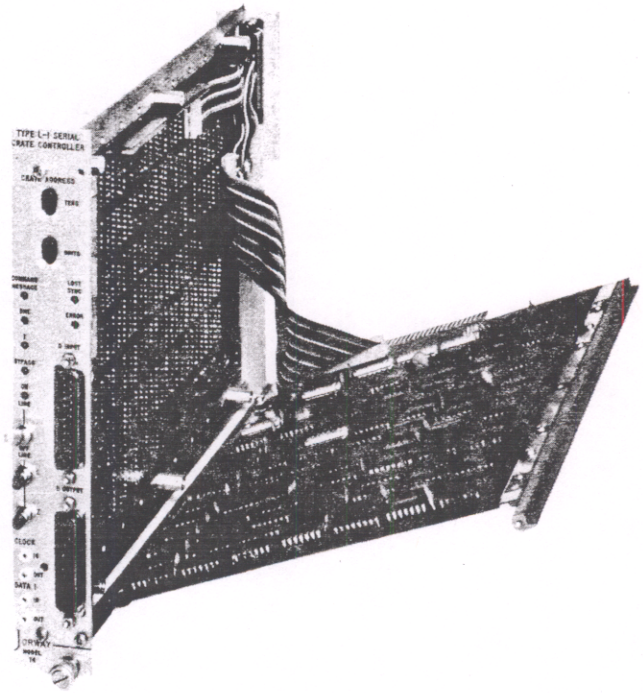
POWER	+6v @ 3200 ma, -6v @ 45 ma
TEMPERATURE	0 to 60 degrees C
MECHANICAL	Two width Camac module with metal side shields.

CONSTRUCTION

The Model 74 is constructed as a two width module which occupies the control station and adjacent normal station in the crate, thereby having access to all Dataway lines.

The two main circuit boards utilize an advanced technology which replaces the usual printed circuitry. Through the use of this process, unusually high component densities are achieved. Basically, the "Multiwire" process is a system in which a pattern of insulated wires are laid down on both sides of an adhesive coated glass-epoxy substrate by a machine operating under numerical control. The wires connect to component holes in the substrate in much the same manner as printed traces. The wire ends are actually embedded in the plated through holes providing extremely reliable connections. The entire wire pattern is then covered with a protective thin epoxy overlay. The substrate itself contains the power and ground busses and connector fingers which are formed by the usual etched printed circuit process. Finally, the whole assembly is cured to bond the layers into a rugged circuit board. Component replacement, if necessary, is accomplished with the same techniques used with conventional printed circuit boards.

In the design of the Model 74, particular emphasis was placed on making the unit easily accessible for servicing if required. All interconnections between the two main boards are by a system of mating headers and sockets. Thus, the two boards can be separated without disconnecting any soldered connections (see picture at right). The front panel components are mounted on a circuit board behind the panel which is connected to the main circuitry by a plug and socket arrangement permitting the front panel to be easily removed.



View of Model 74 with right hand circuit board pivoted outward to facilitate inspection or replacement of components.